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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,640	.01/16/2004	Craig Chaiken	16356.841 (DC-05832)	1223

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,640	CHAIKEN ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5-17-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

It does not identify the citizenship of each inventor.

It does not identify the city and either state or foreign country of residence of each inventor. The residence information may be provided on either an application data sheet or supplemental oath or declaration.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 10-19 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,347,202 to Shishizuka et al., in view of U.S. Patent 5,471,625 to Mussemann et al.

5. As to claim 1, Shishizuka discloses a method for allowing a processor to enter low power states in an information handling system (IHS), the method comprising: detecting an access request for a bus mastering device [FIG. 88]; and in response to failing to detect an access request for the bus mastering device within a predetermined period of time, suspending a bus mastering device controller [FIG. 88].

Shishizuka teaches the limitations of the claim, but does not teach suspending a bus mastering device controller associated with the bus mastering device, wherein the now suspended controller no longer prevents the processor from entering low power states.

Mussemann teaches that operation of a bus mastering device [16] can be suspended [col. 5, lines 30-40] by a bus mastering device controller [14]. Thus, Mussemann teaches a bus mastetering device that can enter a low power mode similar to that of Shishizuka. Mussemann further teaches that the bus mastering device controller can prevent a processor from enter a low power state when [col. 3, lines 39-49], and that it no longer prevents such a transition when the processor can enter the low power state [col. 6, lines 13-28].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the processor low power state control means as taught by Mussemann. One of ordinary skill in the art would have been motivated to do so that the processor does not prematurely enter a low power state if it is needed for operation.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of a system comprising bus mastering device controller associated with the bus mastering device entering a low power state. Moreover, the processor low power state control means taught by Mussemann would improve the power conservation of Shishizuka because it allowed for the power mode of the processor to be controlled [col. 1, lines 46-67].

6. As to claim 2, Shishizuka discloses starting a timer for the predetermined period of time [FIG. 88]; and in response to failing to detect an access request for the period of time, expiring the timer, wherein suspending the bus mastering device controller is performed in response to the timer expiring [FIG. 88].

7. As to claim 3, Shishizuka discloses in response to detecting an access request for the bus mastering device, restarting the timer for the predetermined period of time [FIG. 88].

8. As to claim 4, Shishizuka discloses in response to detecting an access request for the bus mastering device, also resuming operation of the bus mastering device controller if the bus mastering device controller has been suspended [FIG. 88].

9. As to claim 5, Shishizuka discloses detecting an access request for the bus mastering device includes detecting an input/output request packet (IRP) [FIG. 88].

10. As to claims 6-7, Shishizuka discloses detecting an access request for the bus mastering device, starting the timer for the predetermined period of time, and resuming the operation of the bus mastering device controller are performed in response to an executable code executable by the IHS [FIG. 88]. Furthermore, it is well known in the art that a filter driver is executable code used to control hardware devices within a computer system.

11. As to claims 10-13, Mussemann discloses the system comprises a bus mastering device for a bus that provides for communication between different systems within a computer [col. 1, lines 14-44]. In addition, Shishizuka teaches that a bus in a computer system may be a USB [FIG. 4]. Furthermore, USB bus devices such as a floppy disk drive and an optical disk drive are well known in the art.

12. As to claim 14, Shishizuka discloses an information handling system (IHS) comprising: a processor [401] capable of entering low power states, a memory coupled to the processor [403]; a non-volatile storage, coupled to the processor [403]; a bus mastering device [5501]; a bus mastering device controller coupled to the bus mastering device and the processor, for transferring information between the bus mastering device and the processor [5502]; and an executable code stored in the non-volatile storage for detecting an access request for the bus mastering device and causing the bus mastering device controller to be suspended in response to failing to detect an access request for the bus mastering device within a predetermined period of time [FIG. 88]. Mussemann further teaches that the bus mastering device controller can prevent a processor from enter a low power state when [col. 3, lines 39-49], and that it no longer prevents

such a transition when the processor can enter the low power state [col. 6, lines 13-28]. Mussemmann also teaches that the bus mastering device [16] can be separate from, and coupled to, the bus mastering device controller [14].

13. As to claim 15, Shishizuka discloses the executable code starts a timer for the predetermined period of time, expires the timer in response to failing to detect an access request for the bus mastering device within the time period, and wherein causing the bus mastering device controller to be suspended is in response to the timer expiring [FIG. 88].

14. As to claim 16, Shishizuka discloses the executable code restarts the timer for the predetermined period of time in response to detecting an access request for the bus mastering device [FIG. 88].

15. As to claim 17, Shishizuka discloses the executable code further causes the bus mastering device controller to resume operation in response to detecting an access request for the bus mastering device, if the bus mastering device controller has been suspended [FIG. 88].

16. As to claim 18, Shishizuka discloses detecting an access request for the bus mastering device includes detecting an input/output request packet (IRP) [FIG. 88].

17. As to claim 19, Shishizuka discloses detecting an access request for the bus mastering device, starting the timer for the predetermined period of time, and resuming the operation of the

bus mastering device controller are performed in response to an executable code executable by the IHS [FIG. 88]. Furthermore, it is well known in the art that a filter driver is executable code used to control hardware devices within a computer system.

18. As to claims 22-25, Mussemann discloses the system comprises a bus mastering device for a bus that provides for communication between different systems within a computer [col. 1, lines 14-44]. In addition, Shishizuka teaches that a bus in a computer system may be a USB [FIG. 4]. Furthermore, USB bus devices such as a floppy disk drive and an optical disk drive are well known in the art.

19. As to claim 26, Shishizuka discloses an information handling system (IHS) comprising: a processor capable of entering low power states, a non-volatile storage, coupled to the processor [FIG. 4]; a bus mastering device [5501]; controller means coupled to the bus mastering device and the processor, for transferring information between the bus mastering device and the processor [5502]; and means stored in the non-volatile storage for detecting an access request for the bus mastering device and causing the controller means to be suspended in response to failing to detect an access request for the bus mastering device within a predetermined period of time, [FIG. 88]. Mussemann further teaches that the bus mastering device controller can prevent a processor from enter a low power state when [col. 3, lines 39-49], and that it no longer prevents such a transition when the processor can enter the low power state [col. 6, lines 13-28]. Mussemmann also teaches that the bus mastering device [16] can be separate from, and coupled to, the bus mastering device controller [14].

20. As to claim 27, Shishizuka discloses a method for allowing a processor to enter low power states in an information handling system (IHS) comprising: providing a processor capable of entering low power states, coupling a non-volatile storage to the processor [FIG. 4]; providing a bus mastering device [5501]; coupling a controller means to the bus mastering device and the processor, for transferring information between the bus mastering device and the processor and limiting the processor from entering low power states [5502]; and storing means in the non-volatile storage for detecting an access request for the bus mastering device and causing the controller means to be suspended in response to failing to detect an access request for the bus mastering device within a predetermined period of time, wherein the now suspended controller means no longer limits the processor from entering low power states [FIG. 88]. Mussemann further teaches that the bus mastering device controller can prevent a processor from enter a low power state when [col. 3, lines 39-49], and that it no longer prevents such a transition when the processor can enter the low power state [col. 6, lines 13-28]. Mussemmann also teaches that the bus mastering device [16] can be separate from, and coupled to, the bus mastering device controller [14].

21. Claims 8-9 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,347,202 to Shishizuka et al., in view of U.S. Patent 5,471,625 to Mussemann et al., in further view of Applicant's Admitted Prior Art.

22. As to claims 8-9, Shishizuka discloses in conjunction with suspending the bus mastering device controller, setting a flag indicating that the bus mastering device controller has been suspended in response to the IHS executing the executable code [FIG. 88]; and resuming operation of the bus mastering device controller if the flag is set [FIG. 88]. In addition, Applicant's Admitted Prior art teaches that the ACPI standard is well known in the art [paragraph 0003]. The ACPI standard further comprises use of flags to indicate power states of devices, as well as SMI protocols.

23. As to claims 20-21, Shishizuka discloses in conjunction with suspending the bus mastering device controller, setting a flag indicating that the bus mastering device controller has been suspended in response to the IHS executing the executable code [FIG. 88]; and resuming operation of the bus mastering device controller if the flag is set [FIG. 88]. In addition, Applicant's Admitted Prior art teaches that the ACPI standard is well known in the art. The ACPI standard further comprises use of flags to indicate power states of devices, as well as SMI protocols.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (571) 272-3671. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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